REMARKS/ARGUMENTS

Claims 1-28 are in the application.

Claim 1 has been rejected under 35 U.S.C. §103(a) over Kitamura et al. (Kitamura), U.S. Patent No. 5,844,275 in view of Ranjan U.S. Patent No. 5,861,657, Sakakibara et al. U.S. Patent No. 5,449,946, and Uenishi et al. (Uenishi), U.S. Patent No. 6,040,600. Reconsideration is requested.

It has been set forth that Kitamura shows all of the features of claim 1 except that it does not show that "the thickness and concentration of said mesas and said diffusions [are] selected to cause each to fully deplete under blocking voltage conditions" as called for by claim 1. It has been set forth, however, that Ranjan at Col. 2, lines 7-16 "discloses a semiconductor device where the mesas and diffusions vary", and thus it would have been obvious to a skilled person to modify the device of Kitamura "to include mesas and diffusions that vary as disclosed in Ranjan because it provides a smaller lateral extent and takes up less chip area."

Col. 2, lines 7-16 of Ranjan provides:

> In the resulting structure, a variation of the depth of top (diffused) resurf region will have a much smaller effect on the charge contained within the pinched region beneath it. This results in a better control over breakdown voltage with a much thinner epitaxial layer for a given breakdown voltage. The thinner epitaxial layer, in turn, reduces the diffusion processing time needed for forming isolation diffusions and the isolation diffusions have a smaller lateral extent and take up less chip area.

Nowhere in the cited excerpt from Ranjan is it taught or suggested to select the thickness and concentration of the mesas and the diffusions on the walls of the mesas "to cause each to fully deplete under blocking voltage conditions" as called for by claim 1. Indeed, the device shown by Ranjan does not include mesas. Furthermore, nothing in Ranjan has been identified to establish that by selecting the thickness and concentration in mesas and diffusions formed in the walls of the trenches as called for by claim 1 smaller lateral extent can be achieved to reduce the chip area taken by the device. It is respectfully submitted that Ranjan does not show or suggest modifying the device shown by Kitamura to obtain a device in which "the thickness and

concentration of said mesas and said diffusions [are] selected to cause each to fully deplete under blocking voltage conditions." Reconsideration is requested.

It has also been set forth that Kitamura shows all of the features of claim 1 except that it does not show that the "mesas extend between said drain and said MOSgate structure." However, it has been set forth that Figure 1 of Uenishi "discloses a semiconductor device where the mesas extend between said drain and said MOSgate structure"; therefore, one skilled in the art, based on the disclosure of Uenishi, could modify the device shown by Kitamura to include mesas that extend between the drain and the gate structure. According to the Office Action, the motivation for such a modification is to obtain a high breakdown voltage.

Referring to Figure 1 of Uenishi, the device shown by Uenishi includes a drain region 4 formed at the bottom of the device and source regions 5 and gate regions are formed on the top of the device. There is no mesa between the drain region 4 and the source region 5 and gate regions 9. If the Examiner disagrees, identification of a mesa as set forth in claim 1 is requested.

Furthermore, there is no evidence in the record to establish that placing the drain of one end of a mesa and the source and gate at the other end of the mesa is known in the art to increase breakdown voltage, thus leading one skilled in the art to modify the device shown by Kitamura to obtain a device according to claim 1. A reference that teaches the motivation for providing a mesa between a drain, and a gate structure as set forth in the Office Action is requested for the record.

It is respectfully submitted that claim 1 is not obvious in view of the cited references for at least the above reasons. Reconsideration is requested.

Claims 2-28 depend from claim 1 and thus include its limitations. Each of claims 2-28 includes additional limitations, which in combination with those of claim 1 are not shown or suggested by the art of record. Reconsideration is requested.

The application is believed to be in condition for allowance. Such action is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 27, 2003:

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Name of applicant, assignee or Registered Representative

Signature

May 27, 2003

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